Claims:

I claim:

1. An electronic control apparatus called for convenience a Field Programmable Instrument Controller (FPIC) for controlling the processes of a process system, said control apparatus comprising:

   a plurality of processing elements each especially adapted to perform special tasks, each said processing elements is a process represented by software programs, or algorithms or by specific hardware elements, namely programmed or firmware-controlled State-Machines and Sequencers or combinatorial asynchronous or sequential Boolean logic circuits, or programmed arrays of gates whereby each said processing element being activated "on the fly" is able to communicate with every other then active processing element;

   a means wherein said process elements operate in parallel or serial manner in plurality of computing architectures instantiated "on the fly" in at least one Field Programmable Gate Array (FPGA) ;

   said computing architectures being of bit size and functionality as defined in a program definition algorithm stored in electronic memory of the said electronic control apparatus for the purpose of embodiment of the architecture in a portion of said FPGA;

   at least one said processing element contained in said control apparatus which has the capability of interfacing to another FPIC or other processor selected from but not limited to members of the group of processors, microcontrollers, microprocessors, or computers; and

   said processing elements which all or severally assume roles needed to create required process control functionality, whereby at least one processing element represents the specific functionality of FPIC memory allocation storage and retrieval, at least one processing element covers all FPIC processing related with interconnected real-time processing and hardware interfaces, at least one processing element exercises all human interfaces, at least one processing element covers FPIC specific functionalities related to controlling processes, and at least one processing element functions as an access point connecting to FPIC external extension units selected from members of the group consisting of but not limited to FPIC, microcontrollers, microprocessors, macroprocessors, FLASH memory, PCMIA, data busses, networks, and communication devices.

2. Electronic control apparatus as in claim 1, wherein one of the processes operating in one or more processors instantiated in said FPIC acts as a common access point.

3. Control apparatus as in claim 1, wherein said processing elements are represented by specific software and hardware elements operating a plurality of individual processors instantiated in said FPIC.

4. Control apparatus as in claim 1, wherein said processing elements are represented by specific hardware elements, namely micro-controller architectures, programmable or firmware-controlled State-Machines and Sequencers or combinatorial asynchronous or sequential Boolean logic circuits instantiated in a plurality of interfaced external electronic control apparatus or processors.

5. Control apparatus as in claim 1, wherein said processing elements are represented by software mapped to a single or to multiple processor architectures instantiated in said FPIC, said software operating asynchronously or synchronously in series or in parallel fashion.

6. A distributed control system for controlling a plurality of processes, the system comprising a plurality of local monitoring devices, having:

   sensors for collecting local data and signals concerning at least one process associated with the monitoring device;

   a local data processor for receiving and communicating the local data from the sensors concerning its associated process;

   a centralized data processor coupled to a plurality of local devices that provide means for monitoring, diagnosing, prognosing and controlling;

   the said centralized data processor providing the means for receiving from each local controlling device the local data concerning its associated process, for generating a set of weighted parameters for each local controlling device, and for communicating the set of weighting parameters to each local controlling device,

   the local processor for each local controlling device further for receiving the set of weighting parameters and processing the local data using the set of weighted parameters for local diagnostic and control purposes, and

   at least one the local controlling devices being one of the electronic control apparatus as in claim 1.

7. The distributed control system as in claim 6 wherein processing elements assume roles, a first control process represents the specific functionality of system support applications, a second control process covers all applications related with real-time networks and direct hardware controls, a third control process exercises all human interface applications and the electronic control apparatus specific functionalities, and a fourth control process functions as a network access point connecting to electronic system external extension units and to local area networks (LAN) or wide area networks (WAN), or wireless networks.

8. The distributed control system as in claim 6 wherein the system support applications are chosen from a group consisting of power management, wake-up and sleep control, system vitality monitor, and system fault handling

9. The distributed control system as in claim 6 wherein the direct hardware is chosen from the group consisting of electronic, electro-mechanical, electro-optic or electro-hydraulic control systems.

10. The distributed control system as in claim 6, wherein the human interface applications are chosen from the group consisting of physical input/output units, visual input/output units and voice input/output units.

11. An electronic control system for controlling the process of a processing system comprising:

    a least one of said control apparatus in communication with a plurality of other electronic processors each of which performs a predetermined function and each of which is able to communicate with remaining ones of said control elements.

12. Control system as in claim 11, wherein the link ports use standard data link protocol and/or the physical representation thereof.

13. Control system as in claim 11, wherein the arbitrated link uses any standard bus access technique.

14. Control system as in claim 11, wherein the control elements are implemented in software operating on processors of said FPIC.

15. Control system as in claim 11, wherein the control elements are implemented using capability of said FPIC in combination capability of other electronic control elements some of which can be another instance of said FPIC.

16. Control system as in claim 11, wherein the tetrahedral interconnection geometry provides simultaneous multi-path communications among control elements.

17. Control system as in claim 11, wherein the tetrahedral interconnection geometry provides real-time capability to electronic control unit (ECU) or central processor unit (CPU) near components, subsystems, and networks.

18. Control system as in claim 11, wherein the tetrahedral interconnection geometry provides secure access to system external units via at least one of a network and wireless connection.